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A Charge-transfer Method and SC Circuit for Measuring Capacitors with One Floating Electrode

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Abstract - **we present a charge transfer method and the switch-capacitor solution for measuring capacitors with one floating electrode. Such principle provides solution for small displacement measurement in industrial environment, where electrical contact with the target is not feasible. The proposed solution is designed to tolerate up to 10-meter cable, and more importantly, due to the special measurement principle, such system is designed to have an improved immunity to external interference even presents with long connection cable. The switch capacitor implementation of active shielding technique is also used to reduce the effect of cable capacitance. The block diagrams of the system and circuit considerations are presented and the simulation results of the system are described.**

Keywords – **capacitive measurement system, long cables, floating electrode.**

I. INTRODUCTION

The principle of capacitive measurement is being used in many industrial applications including measurement of displacement, pressure, acceleration, and liquid level etc. Such measurement principle is popular in industry because it is easy to implement and performs well. The principle of capacitive measurement can be implemented to have a high resolution within short measurement time; meanwhile it can be well-protected from external electromagnetic fields by means of shielding. However, in some industrial applications, possible problem may occur due to the cable connecting the two electrodes of the sensing capacitors sensor from the read-out circuit since the cabling routine is defined in higher level of specification [1]. The cables connecting the sensor with the electronic interface create a loop which acts as an antenna for magnetic fields, thus introducing noise cause by electromagnetic interference. Creating such a closed loop is unavoidable for all interface principles. In some applications, it is not possible so make such connection short and small in area, which creates a challenge in designing such capacitive measurement system.

In this paper, we present a charge-transfer method and switch capacitor circuit realization for the capacitive measurement system used in the above-mentioned circumstance. Both configuration of sensor head and the design of electronic interface will be discussed. The main idea of sensor head configuration is to use a floating electrode to avoid extra electrical contact with the target, which is similar to what is suggested in [2]. And details of electronic interface specify designed for such sensor will be analyzed. Finally the simulation result of the system will be discussed.

II. CAPACITIVE SENSOR WITH ONE FLOATING ELECTRODE

Fig.1 shows the configuration of the sensing capacitor for measuring displacement, which consist of three electrodes, a floating target electrode and the two sensing electrodes, which are equal. The two sensing electrodes are movable and mounted within one single piece of mounting. Such configuration creates two equal sensing capacitor Cxa and Cxb, and they are changing with the same value and direction. Note that this is only for demonstration purpose, other parts of the sensor (like guard rings etc.) are not shown for simplicity.

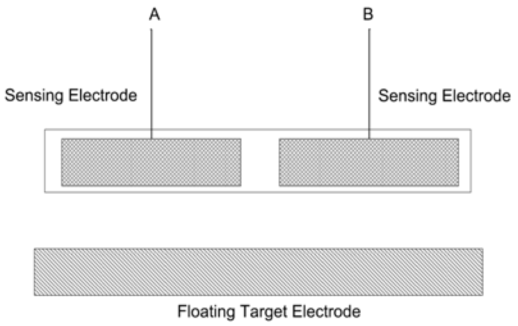

Fig.1 Configuration of the sensor, which consist of two sensing electrode and one floating target electrode. The two connection points (A and B) are on the same side of the sensor head

Doing measurement with such sensor configuration creates two signal loops, as shown in Fig.2. The first loop is the measurement loop, where the measurement current ***i*** is running though. This loop can be implemented using two connection cables that are well shielded from each other. More importantly, since they are located on the same side of the sensor, they can be twisted together and thus make the "effective" loop area small enough regarding to electromagnetic interference. The other loop is the noise coupling loop, since the floating target connects the outside world (ground) via capacitive coupling, producing a parasitic capacitance Cp, from which noise voltage (introduced by potential difference between different ground nodes) injects current to the target. Since the distance between the sensing electrode and the target is much smaller compared with the distance between the

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floating electrode and the outside world (machine body in some application), the value of Cp would be considerably small, which makes the value injected current small. On the other hand, such current is split into two parts by the two signal wires, and which appears as a common mode input signal for the interface electronics. Therefore interface electronics with high CMRR (common mode rejection ratio), can significantly suppress such injected noise.

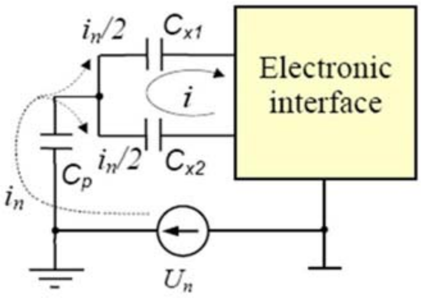

Fig.2 Capacitance measurements using floating electrodes. It consists of two loops, a measurement loop and a noise loop. The noise appears to be common-mode regarding to the signal current and thus can be suppressed by using a front-end with high common-mode rejection ratio

III. ANALYSIS OF ELECTRONIC INTERFACE

A. System Level Consideration

The proposed design is based around a 12 bit ADC which is interfaced to the controlling CPLD/micro-controller and the sensitive analog circuitry. The virtue of such an arrangement will minimize measurement errors and lead to lower component costs, as seen Fig 3. Notice that as well as controlling the ADC, the CPLD controls the analogue switch configuration needed for the capacitance measurement operation. Two reference voltages are also generated locally (±Vref), from the ±15v regulated power supply. Notice that these two references (also used for the capacitance measurement operation) are measured via the ADC to eliminate the influence of the reference.

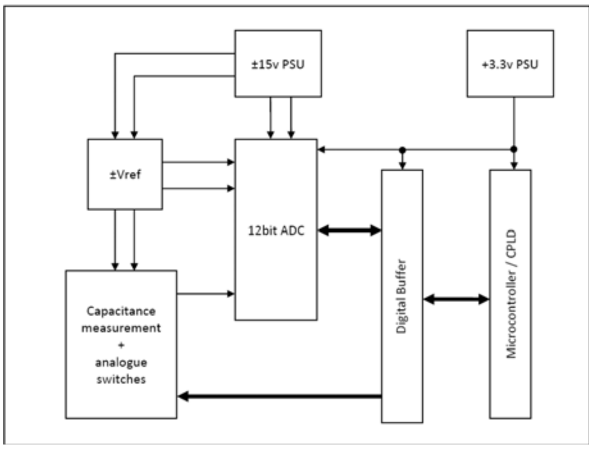

Fig.3 Proposed hardware block diagram, consist of both analog part (the read-out electronics) and digital part (data processing subsystem).

B. Switch capacitor circuit for capacitance measurement

The capacitance measurement circuit is based on "charge-transfer" principle, where the sensing capacitors are charged by the bipolar reference voltage and then the amount of charges are transferred to the voltages by the feedback capacitor across the differential opamp. The basic configuration of the front-end can be seen in Fig. 4, where only half circuit is shown for better demonstration.

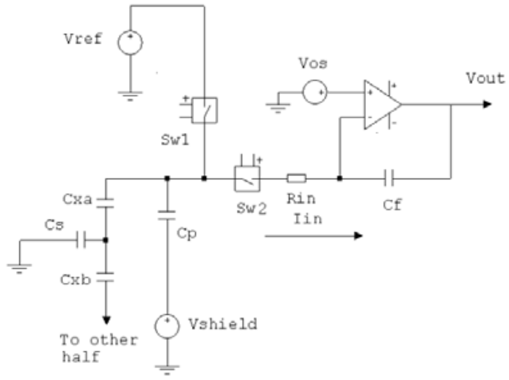

Fig.4. Capacitance measurements circuit based on charge transfer method. Only half circuit is shown for simplicity

Analyzing Fig. 4, it can be seen that the sensing capacitor is Cx (illustrated by Cxa, Cxb is for the identical second circuit and can therefore be ignored for this analysis). One complete measurement cycle consists of four phases. During the first quarter of a cycle, Sw1 is closed and Cx is charged to Vref. During the second quarter of the cycle, Sw1 is opened and Sw2 closed and hence Cx is discharged into the integrator circuit consisting of Rin and Cf connected around an op-amp as shown Fig 2. The third and fourth quarter cycle is the same as the first two, only with the change of polarity of Vref. During the charging cycle, the integrator feedback capacitor Cf is discharged, so that the voltage across Cf starts at zero. Assuming that the op-amp is perfect, Vos can be neglected and V- (i.e. the op-amp’s negative input) is maintained as a virtual ground by the feedback through Cf; then Cx will discharge toward ground through Rin, and Cf will charge so as to maintain V- at ground potential. The charge transfer principle can be described by Eq.1:

$$Cx \times Vref = -Vout \times Cf \tag{1}$$

The current into the op-amp would be (from the formula for the discharge of a capacitor):

$$Iin = \frac{Vref}{Rin}.e^{\left(\frac{-t}{Cx.Rin}\right)} \tag{2}$$

Therefore, assuming the initial voltage on the feedback capacitor is zero:

$$Vout = Vref \cdot \frac{Cx}{Cf} . e^{(\frac{-t}{Cx.Rin})} \tag{3}$$

This is the ideal situation. However, if the op-amp is unable to meet the demands of the initial slew, the effect would be for V- to move slightly more positive than ground, but as the transient proceeded, feedback would restore the virtual earth. Providing that the op-amp input impedance is large, all current must still pass through Cf, and hence the charge transfer relationship would still hold.

The effect of Vos is to produce an error in accuracy. This can be reasoned by applying supposition to the input. Assume that the capacitor has zero voltage initially. Feedback would hold V- at Vos, which would then attempt to charge Cx, by passing current through Cf. This argument, produces an initial “error rate” of:

$$\frac{dVout}{dt} = \frac{Vos}{Cf.Rin} \tag{4}$$

This decay would decay to zero as the voltage on Cx approaches Vos and current into Cx approaches zero. It seems that offset will be an issue in designing the capacitance measurement circuit, but in fact, thanks to the use of four phase measurement with bipolar reference, as well as the other half circuit, offset of the differential integrator op-amp will not affect the final digital output of the measurement result. The final output (digital output) is only sensitive to the difference between the result of the two half circuits, as shown in Eq 5-7:

$$Vout1 = \frac{Cx}{Cf}.Vref + \frac{Cx+Cp}{Cf}.Vos + Vos \tag{5}$$

$$Vout2 = Vos - \frac{Cx}{Cf}.Vref + \frac{Cx+Cp}{Cf}.Vos \tag{6}$$

$$\begin{aligned} Vout &= A.(Vout1 - Vout2) \\ Vout &= 2.A.\frac{Cx}{Cf}.Vref \end{aligned} \tag{7}$$

It can be seen that offset will be cancel out and similar situation also hold for low frequency noise. Moreover, the final digital output, which take the difference of the output in the two half cycles, will be further helpful for such feature.

From the discussion above, we can see that the important parameter to consider would be

1) Op-amp slew rate must be comparable with Vref/Rin in order to ensure no great deviations from virtual ground, i.e. charging of Cf keeps up with discharge of Cx in order to maintain V- at zero volts.

2) Switch charge injection when Sw2 closes is small when compared with Cx.Vos

3) Time constant Cx.Rin is sufficiently small such that Cx has sufficient time to discharge close to zero during the cycle time when sw2 is closed, in order to ensure that adequate accuracy is obtained.

In order to complete the system, two halves of the circuit shown in Fig 4 are required, as the sensing capacitance is split into two identical halves Cxa and Cxb. The measurement cycle consists of two sub cycles, the first with Cxa charged to Vref, and Cxb to –Vref, the second with Cxa charged to –Vref and Cxb to Vref. By using the double ended effect, the current through stray capacitance Cs is held near zero. Also the two measurement sub cycles, with polarities reversed, help combat the effect of accuracy error due to Vos and possible other factors like low-frequency interference.

C. Active shielding technique with switch capacitor approach

Active Shielding technique has been widely used for application that has to deal with long cables [3]. In this application, the connection between the input of the electronics and the sensing capacitance and Cx is via a screened cable with capacitance, Cp. As seen in Fig 4, the voltage on the screen is adjusted by the voltage generator Vshield. During the first quarter cycle Cx is charged to Vref, and Vshield is switched to the same potential. During the next quarter cycle (when Cx is discharged into Rin), Vshield is connected to zero. Providing that the voltage of Vshield matches precisely the voltage across Cx, no current flows to Cx, and the effect of the shield is removed from the measurement. Cp is likely to be much larger than Cx, so a careful consideration of the transient, when Cx discharges is necessary in order to establish the truth or otherwise of this argument.

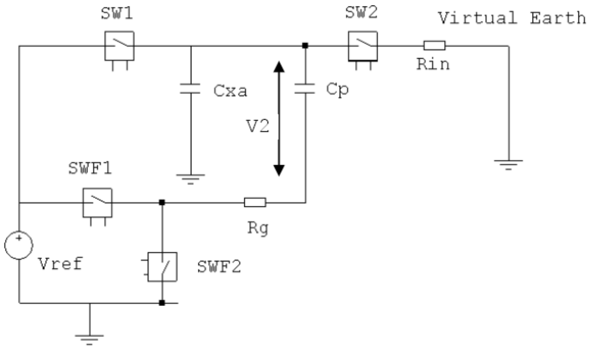

Fig.5 Switch capacitor implementation of the active shielding technique. It only consist of three switches for enabling such function

Analyzing Fig 5, Cxa is the probe capacitance and Cp the capacitance to shield. Cxa is pre-charged to Vref by closing SW1, and the cable capacitance is held at zero volts with respect to Cxa by closing SWF1. During the measurement cycle, SW1 is opened and SW2 is closed so that Cxa is discharged into the virtual earth. Where, SWF2 is closed in an attempt to maintain zero volts across Vref. Unfortunately, Cxa will also discharge into Cp which is now grounded through Rg (represents the resistance of the discharge path into SWF2.) and SWF2. Thus, part of the

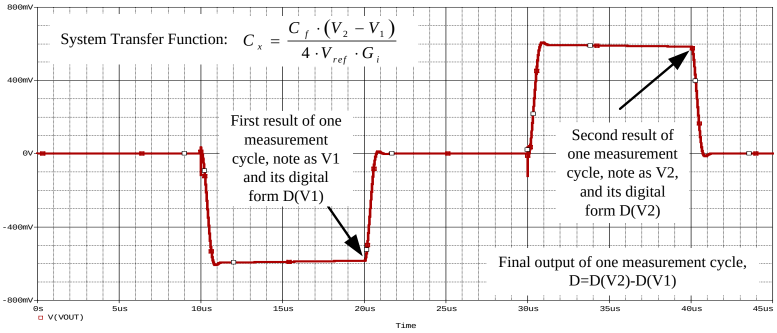

Fig 6**.** Output of the front-end, where critical measurement points and transfer characteristics are indicated. The final output is only sensitive to peak-to-peak value of the two results, which is independent of offset.

charge on Cxa will initially be lost to Cp. The voltage across Cp will still be discharged into Rin, and eventually both Cp and Cxa will reach zero volts.

Let us assume that Rin>>Rg, so initially Cxa discharges into Cp rapidly. Therefore, calculating the voltage (V2) across the shield capacitance, Cp

$$V2 = \frac{Cxa.Vref}{Cxa + Cp} \tag{8}$$

The discharge of Cp into the virtual ground also requires a charge transfer, so for the integrator section:

$$Vout = \frac{Cxa.Vref}{Cf} \tag{9}$$

The output is unchanged. However, the time constant for the transient does change, and consists of the time Cxa+Cp in order to settle to the desired accuracy, by discharging through Rin. However, the voltage V2 is of the order of 50mV, (Cp=100.Cx), so the input signal discharging into the integrator is also fairly small. This makes the effect of Vos much more relevant. Therefore, although the measurement principle makes the result insensitive to offset, low offset would still be beneficial to the system performance.

IV. SIMULATION RESULTS AND PRACTICAL CONSIDERATIONS

The above mentioned circuit has been simulated using circuit models, Fig 6 describe the simulation result for one measurement cycle. The result prove the efficiency of the principle and show that such a system can tolerance up to 10 meter cable, and achieves better immunity to external interference and non-idealities like offset of the component, etc.

Regarding to prototype the system and implementation, several practical aspects should be taken into account.

1) Several low ESR 100F tantalum capacitors are needed on the power supply lines in order to overcome any low/mid frequency interference

2) In order minimize any glitches or erratic behavior due to pickup from external RFI sources, it is recommended to add 100k pull-up resistors to the digital I/O signals in order to increase the board's noise immunity. Also, all signals to and from the external connector should be suitability buffered via a digital buffer, in order to provide protection and ensure consistent startup behavior.

3) Analog switches EMC/ESD protection. A suitable protection scheme should be devised for protecting the delicate CMOS analogue inputs from ESD (electrostatic discharge) or RFI (radio frequency interference), when connected to the 10m cable. We feel that this should be reinforced with an external clamp.

V. CONCLUSION

In this article, the system level and circuit level design of capacitive measurement system is presented. Such system enables the feasibility of measuring capacitor with one floating electrode. Detailed analyses as well as the simulation result have proven the effectiveness of such measurement principle. On the other hand, the switch capacitor approach for active shielding prevent the system to have problem when presents with long cable. Practical considerations are also discussed to ensure that the prototype will work as intended. The future focus of the project will be the experimental result of the prototype and further development of the concept.

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